Integrated device for microfluid thermoregulation, and manufacturing process thereof

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Cited Documents: US5716842; GB2325464; US5690841; US5429734

Abstract

The integrated device (1) for microfluid thermoregulation comprises a semiconductor material body (2) having a surface (3); a plurality of buried channels (4) extending in the semiconductor material body (2) at a distance from the surface (3) of the semiconductor material body (2); inlet and outlet ports (5a, 5b) extending from the surface (3) of the semiconductor material body (2) as far as the ends (4a, 4b) of the buried channels (4) and being in fluid connection with the buried channels; and heating elements (10) on the semiconductor material body. Temperature sensors (15) are arranged between the heating elements (10) above the surface (3) of the semiconductor material body (2).

Description

[0001] The present invention refers to an integrated device for microfluid thermoregulation and a manufacturing process thereof.

[0002] As is known, the treatment of some fluids involves an increasingly precise temperature regulation, in particular when chemical or biochemical reactions are involved. Furthermore frequently the need is felt of using very small amounts of fluid since the fluid is costly or not readily available.

[0003] This is, for example, the DNA amplification process (Polymerase Chain Reaction process, or PCR process) in which precise temperature control in the various steps (it is necessary to perform repeated preset thermal cycles), the need to avoid as far as possible thermal gradients in the fluid reaction areas (so that in these areas there may be a uniform temperature), and also the quantity of fluid used (which is very costly) are of crucial importance for obtaining a good reaction efficiency or even for obtaining the reaction itself.

[0004] Other examples of fluid treatment having the above characteristics are, for example, linked to the performance of chemical and/or pharmacological analyses, biological tests, etc.

[0005] At present, various techniques are available that enable thermal control of chemical or biochemical reagents. A first technique uses a reactor including a glass or plastic base on which a biological fluid is deposited by a pipette. The base rests on a hot-plate called "thermo-chuck", which is controlled by external instrumentation.

[0006] Another known reactor includes a heater, which is controlled by appropriate instrumentation and on which a biological fluid to be examined is deposited. The heater is supported by a base also carrying a sensor set in the immediate vicinity of the heater and is also connected to the temperature regulation instrumentation, so as to enable precise temperature control.

[0007] Both types of reactors are often enclosed in a protective casing.

[0008] A common disadvantage of the above known reactors lies in the large thermal mass of the system; consequently, they are slow and have high power absorption. For example, in case of the PCR process mentioned above, times of the order of 6-8 hours are required.

[0009] Another disadvantage of known solutions is linked to the fact that they are able to treat only relatively high volumes of fluids (i.e., minimum volumes of the order of millilitres) because of the macroscopic dimensions of the reactors.

[0010] The above disadvantages result in very high treatment costs (in the case of the aforementioned PCR process, the cost can amount to several hundreds of dollars); in addition, they restrict the application of known reactors to test laboratories alone.

[0011] A recent solution (see, for example, patent US-A-5,858,195) describes a microchip laboratory system and method that enable manipulation of a fluid for a plurality of applications including injection of samples for chemical separation. The microchip is manufactured using standard photolithographic procedures and by etching a substrate, preferably of glass, on which surface channels are made and which is bonded directly on a covering plate. Also envisaged is the use of a silicon substrate.

[0012] The aim of the invention is therefore to provide a reactor for carrying out chemical, biochemical or pharmacological reactions on small quantities of fluid, which is able to furnish precise thermoregulation.

[0013] According to the present invention an integrated device for microfluid thermoregulation and a manufacturing process thereof are provided, as defined in Claims 1 and 7, respectively.

[0014] In practice, an integrated microreactor is provided which exploits the mechanical properties of semiconductor materials, and in particular of silicon. The microreactor can be manufactured using steps that are standard in microelectronics, and enables fluids to be contained and/or circulated in

microchannels, if necessary mixed with appropriate reagents, as well as treated with heat, possibly repeated according to preset cycles, at precisely controlled temperature and duration.

[0015] For a better understanding of the present invention, preferred embodiments thereof are now described, as nonlimiting examples, with reference to the attached drawings, wherein:

Figure 1 is a perspective view of a base incorporating a first embodiment of the integrated device for thermoregulation according to the invention;
Figure 2 shows a perspective cross-section of the integrated device of Figure 1, taken along section line II-II of Figure 1;
Figure 3 is a perspective cross-section of the integrated device of Figure 1, taken along section line III-III of Figure 2;
Figure 4 shows a perspective view similar to that of Figure 1, for a second embodiment of the thermoregulation integrated device according to the invention;
Figure 5 shows a cross-section of a semiconductor wafer in a first manufacturing step of the device of Figure 1;
Figures 6-11 illustrate cross-sections of a part of the wafer of Figure 5, in subsequent manufacture steps; and
Figures 12-14 show longitudinal sections, perpendicular to those of Figures 6-11 and at an enlarged scale, in subsequent manufacture steps.

[0016] Figures 1-3 show an integrated device 1 comprising a body 2 of semiconductor material, typically monocrystalline silicon, having a surface 3 and parallelepiped shape. The body 2 is traversed by a plurality of channels 4 (visible in the sections of Figures 2 and 3) connected to the surface 3 of the body 2 through an inlet port 5a and an outlet port 5b, which are connected to the channels 4 at ends 4a and 4b of the channels 4. Heating elements 10 are present on the surface 3 of the body 2.

[0017] In detail, the channels 4 extend parallel to each other, in the lengthwise direction of the body 2, at a preset distance from the surface 3. For example, for the use of the device as a reactor in the DNA amplification process, the channels 4 may have a roughly circular or rectangular section, may be spaced 50 mu m, and may be set at a depth of 5-10 pm from the surface 3. In the case of rectangular section, the channels 4 have a side of approximately 30 x 200 mu m and occupy an area of 5 x 10 mm.

[0018] In Figures 1-3, the channels 4 are all connected to a same inlet port 5a and to a same outlet port 5b, and are thus in parallel. The inlet port 5a and outlet port 5b have an elongated shape and extend perpendicularly to the channels 4 and to the surface 3, at the two opposite ends of the channels 4.

[0019] In the embodiment of Figure 4, the channels 4 are spaced from each other and have respective inlet ports 12a and respective outlet ports 12b, which extend perpendicular to the channels 4 and to the surface 3. The inlet ports 12a are preferably aligned and connected to a first end 4a of the channels 4, and the outlet ports 12b are aligned and connected to a second end 4b of the channels 4.

[0020] The heating elements 10 are formed, as been mentioned, on the surface 3 of the body 2 and are insulated from the body 2 by an electrically insulating material layer 17, for example of silicon dioxide.

[0021] Each of the heating elements 10, which are four in number in the illustrated embodiment, comprise a rectangular region that extends transversely with respect to the extension of the channels 4, and the heating elements 10 are adjacent to each other so as to practically cover the entire portion of the surface 3 overlying the channels 4, except for intermediate strips 11 of the surface 3. Each of the heating elements 10 is connected by two electric connection regions 13 arranged on the opposite shorter sides of each of the heating elements 10.
As illustrated in Figure 1, sensor elements 15 extend above the intermediate strips 11 of the surface 3, and include for example coil-shaped metal regions that are represented schematically and are connected at their ends to contact regions 16. The sensing elements 15 are of a material having a resistance varying sensibly upon the temperature and are connected to a resistance sensing circuit of known type, for example of bridge type, not illustrated and preferably formed in the body 2.

[0022] In a way which is not illustrated, the body 2 may integrate electronic components for controlling the temperature and/or for processing the signals picked up by the integrated device.

[0023] In use, the liquid to be treated and/or to be made to react with a reagent is introduced from a reservoir located above the integrated device 1 through the inlet port 5a or the inlet ports 12a, is forced to flow through the channels 4, and is possibly mixed with appropriate reagents at a controlled temperature. The heating elements 10 maintain a controlled temperature throughout the channel area; in particular, because of its micrometric dimensions, the entire channel area 4 is evenly heated, and there is no temperature gradient along and across the channels 4 themselves.

[0024] According to the treatment to be carried out, it is possible to perform a series of heat cycles, each time controlling the'temperature with precision as desired for a preset time by virtue of the temperature sensors 15 cooperating with a suitable control system of known type.

[0025] The treated and/or reacted liquid exits the integrated device 1 through the outlet port 5b or the outlet ports 12b.

[0026] An example of a manufacturing process for the integrated device 1 will now be described with reference to Figures 5-14.

[0027] As illustrated in Figure 5, a hard mask 25 is initially formed on the surface 22 of a wafer 21 of semiconductor material, for example silicon, using processing steps known in microelectronics; the hard mask 25 comprising overlying oxide regions 23 and nitride regions 24, which delimit between each other elongated ports extending perpendicularly to the drawing plane.

[0028] Subsequently, using the hard mask 25, the wafer 21 is etched (first trench etch), so as to form trenches 26 (Figure 5) having a width, for example, of between 0.2 and 3 mu m, and a depth of, for example, between 20 and 30 mu m. The trenches 26 are preferably parallel to one another and spaced 1-30 mu m.

[0029] Subsequently, as shown in Figure 6, the wafer 21 is oxidized to form an oxide layer 27 having a thickness, for instance, of approximately 20 nm, which covers the walls 26a and bottom 26b of the trenches 26 and joins the oxide portions 23, so as to form a single layer. In the illustrated embodiment, a nitride layer 28 is then deposited having a thickness of between 90 and 150 nm, joining the nitride portions 24, to form a single layer. The second nitride layer 28, however, is not indispensable.

[0030] Subsequently (Figure 7), the nitride is dry etched and the oxide is dry or wet etched. The horizontal portions of the nitride layer 28 and oxide layer 27 as well as the horizontal portions of the second nitride layer 28 on the surface 3 of the wafer 21 are so removed from a bottom 26b of the trenches 26, so forming spacers 30 on walls 26a of the trenches 26 and leaving the monocrystalline silicon bare on the bottom 26b of the trenches 26. The hard mask 25 remains on the surface 3 of the wafer 21.

[0031] Next (Figure 8), silicon is etched beneath the trenches 26 for a given time using tetramethyl ammonium hydroxide (TMAH). Alternatively, an isotropic etch may be carried out. Thus the channels 4 are formed, which have a much greater width than the trenches 26.

[0032] Subsequently (Figure 9), the walls of the channels 4 are coated with an inhibiting layer 31, which does not allow epitaxial growth. For this purpose, for instance, a fast oxidation step may be carried out, so as to grow an oxide layer (having a thickness greater than that of the oxide portions 23 and 27 that coat the surface 3 of the wafer 21 and the wall 26a of the trenches 26, as explained later, for example a thickness of between 60 and 100 nm), or else a layer of a material chosen among deposited oxide, nitride and tetraethyl orthosilicate (TEOS) may be deposited in a similar way. Alternatively, the inhibiting layer 31 may be dispensed with, as explained hereinbelow.

[0033] Next (Figure 10), the first spacers 30 are removed from the walls 26a of the trenches 26, and the hard mask 25 is removed from the surface 3 of the wafer 21. During removal of the oxide portions 26 and 27, also part of the inhibiting layer 31 is removed, which, however, being thicker, as mentioned above, is not removed completely and remains to a sufficient extent to guarantee complete coverage of the walls of the channels 4.

[0034] Subsequently (Figure 11), an epitaxial layer 33 is grown, using the monocrystalline silicon of the wafer 21 as nucleus. Consequently, monocrystalline silicon grows horizontally inside the trenches 26, so

closing them, and vertically starting from the surface 3 (which is no longer illustrated in Figure 11). If the inhibiting layer 31 is present, it inhibits growth of the silicon inside the channels 4 in such a way that the latter maintain their original dimensions determined by the timed TMAH etching. If, instead, the inhibiting layer 31 is not present, the channels 4 partially close. This may be advantageous in the case where the exact dimensions of the channels 4 are not very important, and it is preferred, instead, not to have any material other than silicon on the walls of the channel 4.

[0035] In this way, a monolithic monocrystalline-silicon wafer 35 is obtained, including the substrate 21 and the epitaxial layer 33, and housing completely closed channels 4, which are delimited internally by the inhibiting layer 31.

[0036] In a way that is not shown, inside the wafer 35 conductive and/or insulating regions may be formed for manufacturing integrated electrical components belonging to control circuits and/or circuits for processing signals required for the operation of the thermoregulation device 1.

[0037] Subsequently (Figure 12), on the surface 36 of the wafer 35 an insulating layer 37, for example of silicon dioxide, is formed. The insulating layer 37 has, for example, a thickness of 200-300 nm so as to have a reduced thermal resistance. Next, using a trench mask (not shown), the inlet ports 5a or 12a and outlet ports 5b or 12b are formed (Figure 13). Finally, the heating elements 10 are formed, for example a polycrystalline silicon layer is deposited and defined photolithographically (Figure 14).

[0038] Before or after forming the heating elements 10, on the wafer 35 conductive and/or insulating regions are formed as necessary for manufacturing integrated electronic components, not shown. Further steps then follow including depositing and defining metal layers to form metal connection regions 13, the sensing elements 15, and electric connection lines, as well as any other steps required for forming service layers. Finally, the wafer 35 is fixed to a silicon cover wafer (not shown) containing reservoirs and further elements necessary for the desired application, and the assembly is then cut into individual dice.

[0039] The integrated device 1 has the following advantages:

it has a very small thermal mass as compared to present solutions, thanks to its micrometric dimensions and to the physical characteristics of monocrystalline silicon wherein the channels 4 are formed; consequently, it is possible to rapidly heat or cool the fluid flowing in the channels 4, with considerable reduction in the process times;
it requires a very small operating power as compared to known solutions;
the manufacturing costs are much reduced and comparable with current integrated devices;
the treatment costs are much lower than presently, since the device according to the invention enables treatment of very small amounts of fluid (i.e., in the region of microlitres instead of millilitres), and it is possible to achieve better performance of the chemical reactions thanks to the reduced path of the reagents;
the possibility of integrating both the control electronic devices and the processing electronic devices in a same semiconductor material body enables, on the one hand, a very precise control of the treatment conditions and, on the other, a further reduction in costs;
it is possible to manufacture portable analysis devices and disposable devices for performing analyses and treatments where it is essential to prevent contamination from fluids that do not belong to a same sample;
the thermoregulation device can be made in an easily reproducible way, thanks to the use of well-known and controllable manufacturing technologies;
since the channels 4 are buried inside the semiconductor wafer 35, they are not exposed to the external environment, even before fixing a covering element, and hence are less subject to possible contamination, for example due to subsequent manipulation and/or to the glue used for fixing the covering element;
the presence of channels 4 in the wafer 35 of semiconductor material and heating elements 10 on the surface of the wafer 35 with the interposition alone of insulating layers (insulating layer 37) yields a complete uniformity of temperature at the channels 4; consequently, during operation, no significant differences in temperature exist either between adjacent channels or along or across each channel 4; in practice, any point inside the channels 4 has the same temperature as the others, as is essential in particular applications, such as the process of DNA amplification; and
given the ease of processing of the silicon, substrate 21, it is moreover possible to make channels 4 having the desired shape and dimensions.

[0040] Finally, it is clear that numerous variations and modifications may be made to the device and to the manufacturing process described and illustrated herein, all falling within the scope of the invention, as defined in the attached claims. For example, instead of having a plurality of channels 4, the thermoregulation device 1 may comprise a single buried channel of a suitable width, and the trenches 26 may be set at a distance whereby, in the subsequent timed TMAH etching for forming the channels 4, the silicon between the channels 4 themselves is removed completely.

Claims

1. An integrated device (1) for microfluid thermoregulation, characterized by:

a semiconductor material body (2) having a surface (3);
at least one buried channel (4) extending in said semiconductor material body (2), arranged at a distance from said surface (3), and having a first and a second end (4a, 4b);
at least one first port (5a; 12a) and one second port (5b; 12b) extending from said surface (3) respectively as far as said first end (4a) and second end (4b) of said buried channel (4), and being in fluid connection with said buried channel; and
at least one heating element (10) arranged on said semiconductor material body.

2. The device (1) according to Claim 1, characterized by a plurality of buried channels extending parallel and adjacent to each other.

3. The device (1) according to Claim 2, characterized in that said inlet port (5a) and said outlet port (5b) are connected to all said buried channels (4).

4. The device (1) according to Claim 2, characterized by a plurality of inlet ports (12a) and a plurality of outlet ports (12b), said inlet and outlet ports extending from said surface of said semiconductor material body to a respective end (4a, 4b) of a respective buried channel (4).

5. The device (1) according to any of the foregoing claims, characterized by a plurality of heating elements (10) extending adjacent to each other, and each having opposite electric connection regions (13) arranged on opposite sides of said buried channel (4).

6. The device (1) according to Claim 5, characterized by a plurality of temperature sensing elements (15) arranged between pairs of adjacent heating elements (10).

7. A process for manufacturing an integrated device for microfluid thermoregulation, characterized by the steps of:

forming a semiconductor material body(2) having a surface (3);
forming at least one buried channel (4) extending in said semiconductor material body (2), arranged at a distance from said surface (3), and having a first and a second end (4a, 4b);
forming at least one first and one second port (5a, 5b; 12a, 12b) extending from said surface (3) respectively as far as said first (4a) and second ends (4a, 4b) of said buried channel (4), and being in fluid connection with said buried channel; and
forming at least one heating element (10) on said semiconductor material body.

8. The process according to Claim 7, characterized in that said steps of forming a semiconductor material body and forming at least one buried channel comprise the steps of:

forming a substrate of semiconductor material (21);
forming surface trenches in said substrate; and
growing an epitaxial layer on said substrate.

9. The process according to Claim 8, characterized in that, after forming surface trenches and before growing an epitaxial layer, said substrate (21) is anisotropically etched beneath said surface trenches (26) to form said channels (4).

10. The process according to any of Claims 7-9, characterized by depositing an insulating material layer on said semiconductor material body, before forming at least one heating element (10).

11. The process according to any of Claims 7-10, characterized by the step of forming at least one thermosensing element (15) on said semiconductor material body (35), adjacent to said heating element (10).

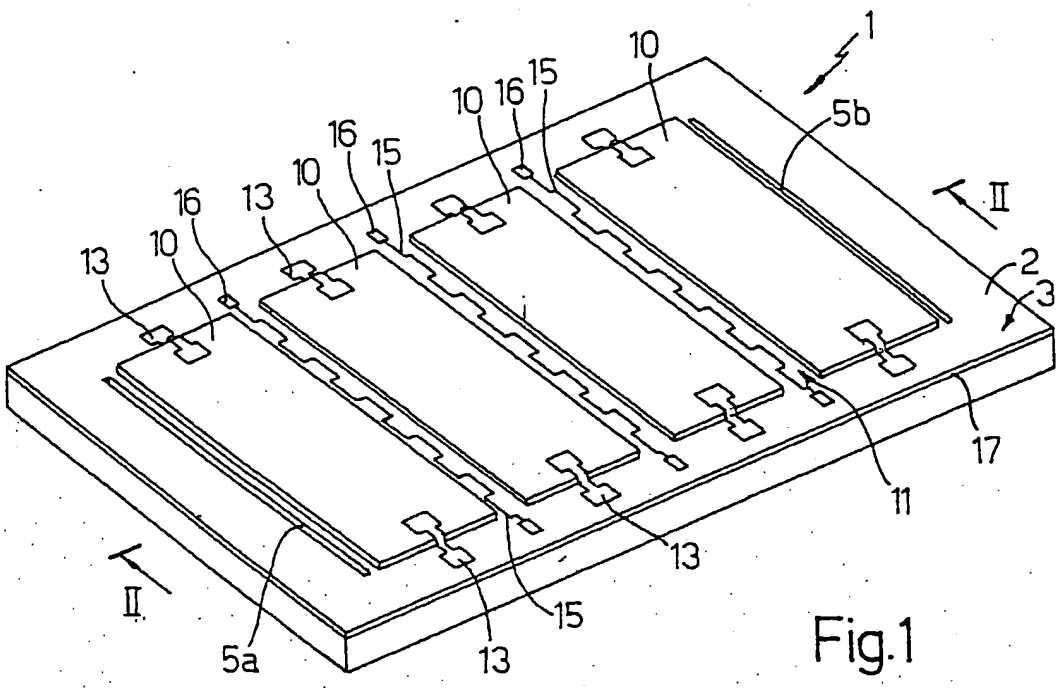
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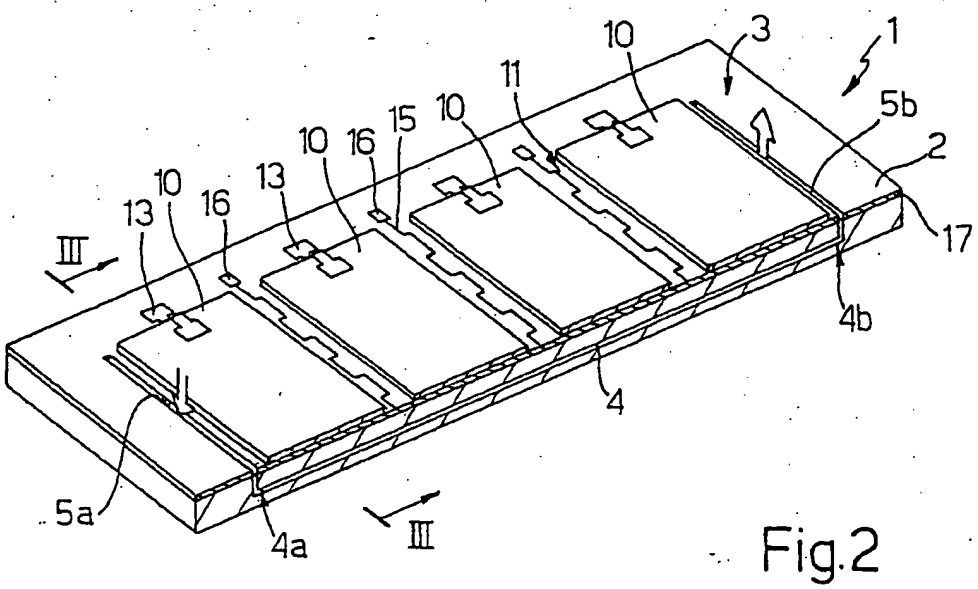
Fig.1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III

Fig.2

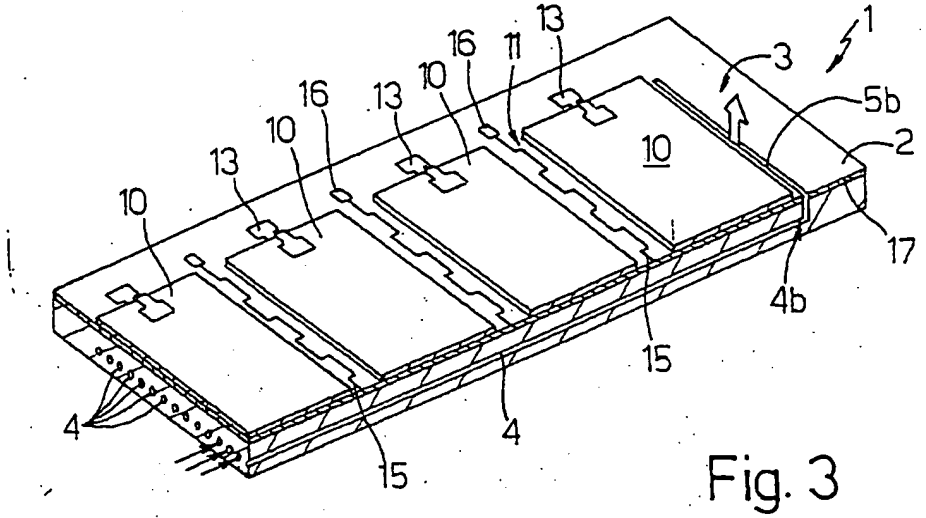

Fig. 3

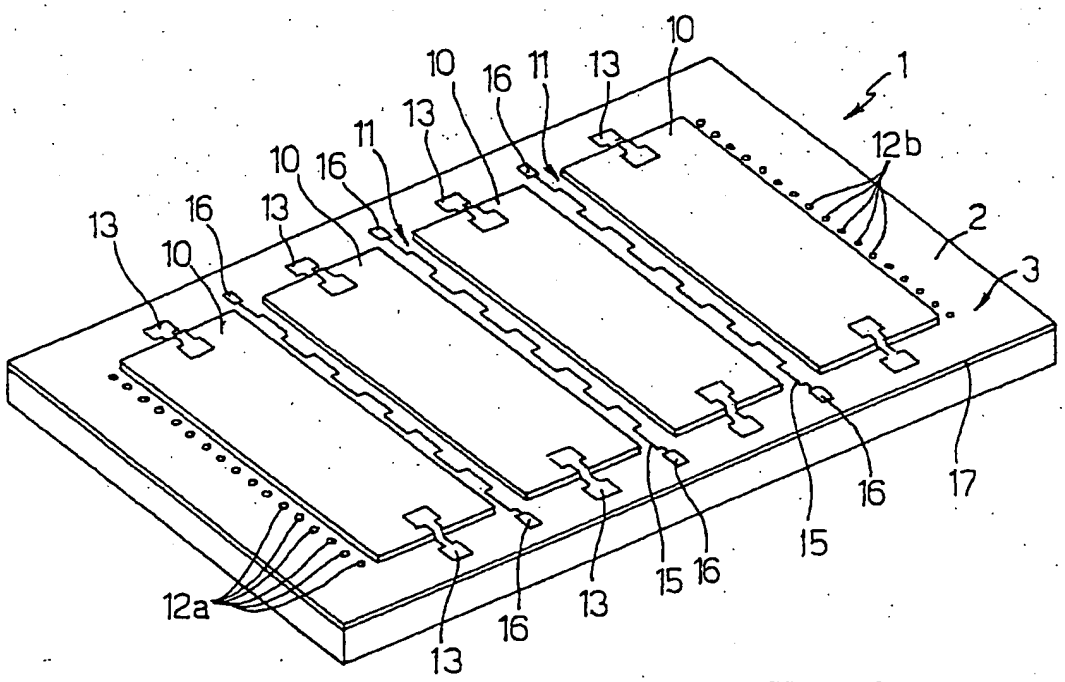

Fig.4

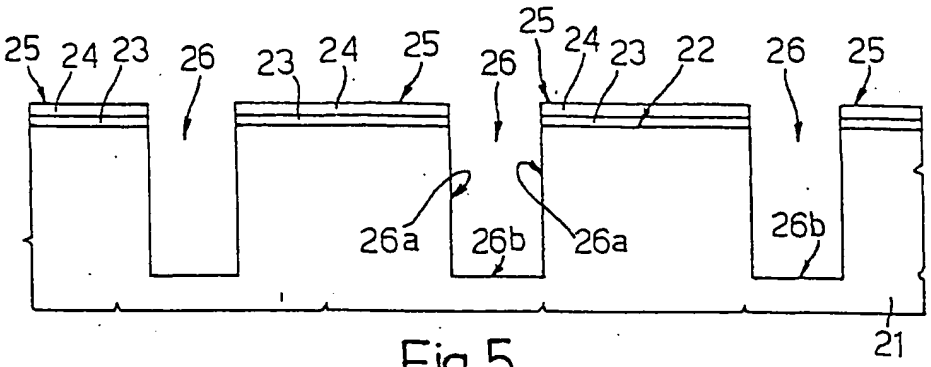

Fig.5

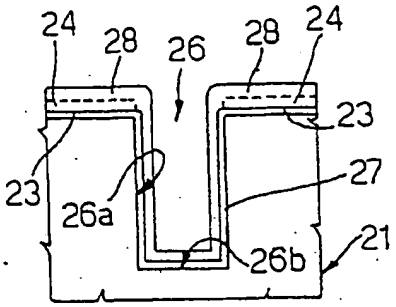

Fig.6

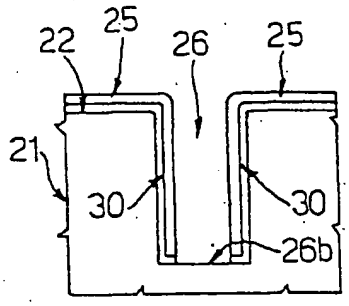

Fig.7

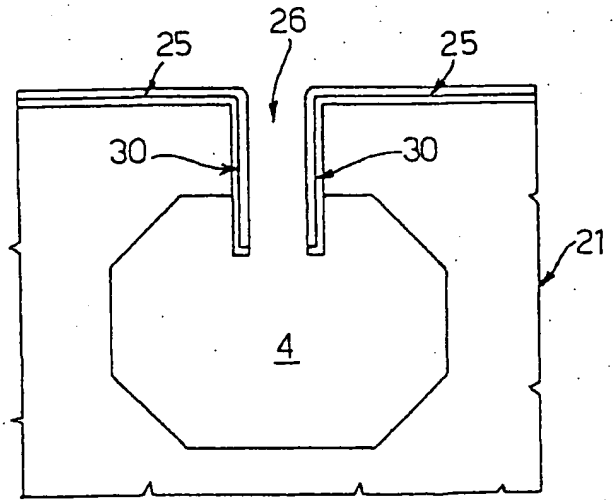

Fig.8

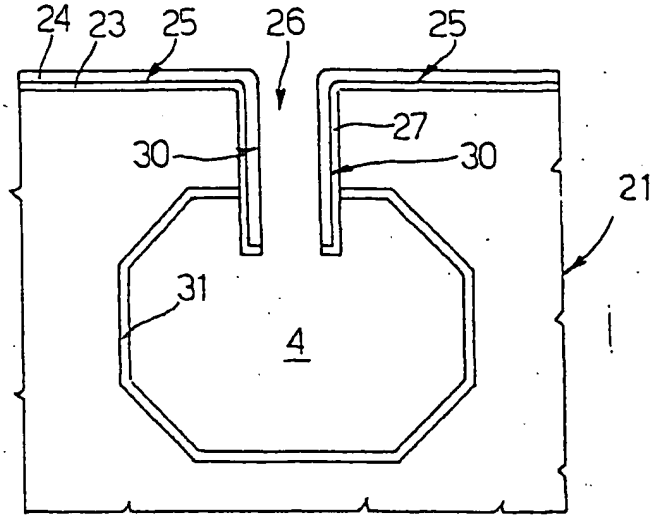

Fig.9

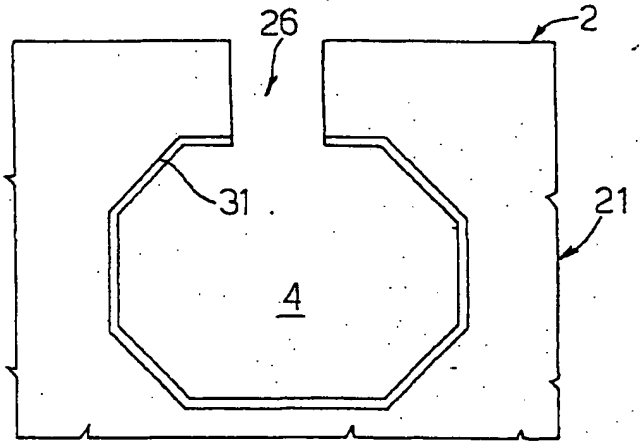

Fig.10

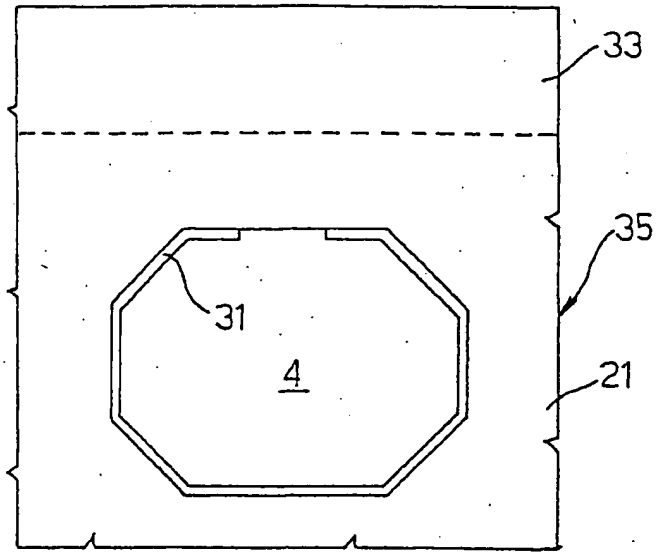

Fig.11

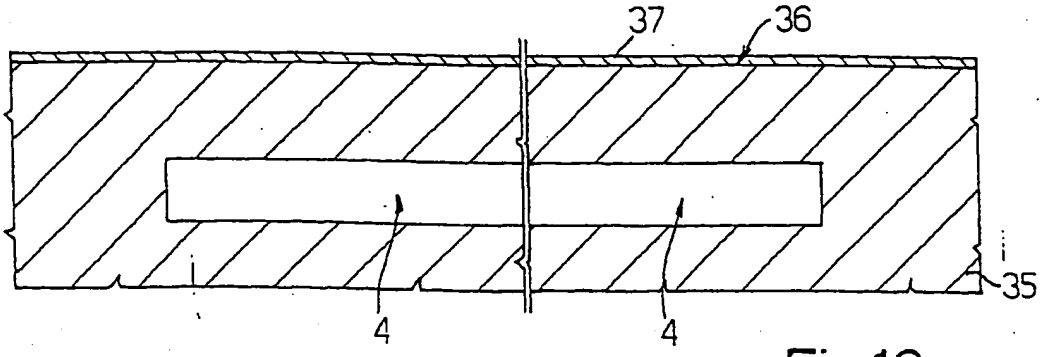

Fig.12

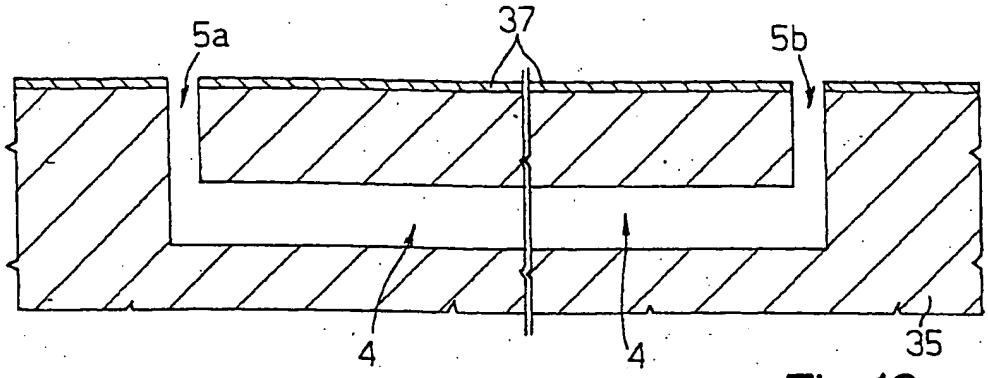

Fig.13

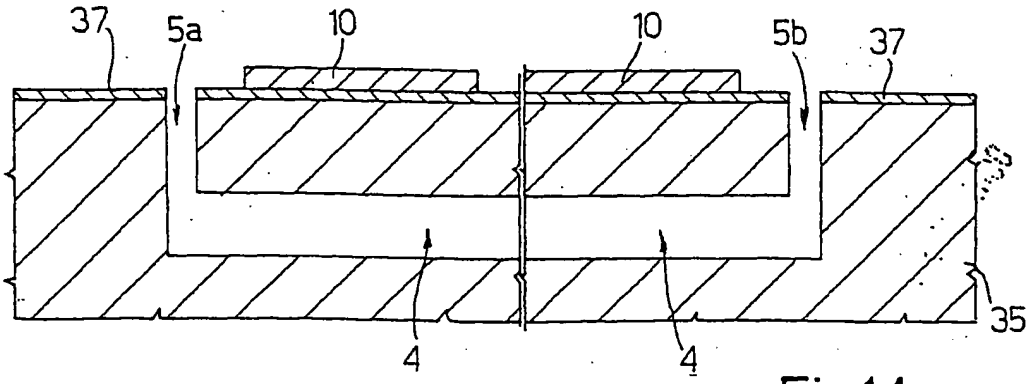

Fig.14